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PATENT & TRADEMARK

2185-#6  
BT  
Patent  
Docket No.: CYPR-CD00229 3-5-03

# Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.			
Date of Deposit:	02/24/03	Name of Person Making the Deposit:	KATHERINE RINALDI
		Signature of the Person Making the Deposit:	<i>Katherine Rinaldi</i>

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Harold Kutz and Warren Snyder      Group Art Unit:  
Filed: 06/22/01      Examiner:  
Serial No.: 09/887,923  
Title: NOVEL METHOD AND SYSTEM FOR INTERACTION BETWEEN A PROCESSOR AND A POWER ON RESET CIRCUIT TO DYNAMICALLY CONTROL POWER STATES IN A MICROCONTROLLER

The Commissioner of Patents and Trademarks  
Washington, D.C. 20231  
Sir:

### Information Disclosure Statement Transmittal

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Transmitted herewith is the following:

- ..... Formal drawings, totaling ..... sheets.
- ..... Informal drawings, totaling ..... sheets.
- ..... Certification for PTO Consideration
- ..... Information Disclosure statement (\_\_\_ sheets)
- ☒ Information Disclosure statement and late filing fee
- ☒ Form 1449
- ..... Petition for Extension of Time
- ☒ Other: REFERENCES
- ☒ Other: Related Pending Us Patent Applications

Fee Calculation (for other than a small entity)				
Fee Items			Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere)			\$ .00	\$0.00
Information Disclosure Statement, late filing			\$180.00	\$0.00
Other:				\$0.00
Total Fees				\$0.00

## PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:
  - [X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.  
A duplicate copy of this authorization is enclosed.
  - [ ] A check in the amount of \$
  - [ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

**WAGNER, MURABITO & HAO LLP**  
Two North Market Street, Third Floor  
San Jose, California 95113  
(408) 938-9060

Respectfully submitted,

Date:

2/24/2003

By:



Anthony C. Murabito  
Reg. No. 35,295



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00229

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Washington, D.C. 20231

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

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The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
5,734,272	DIFFERENTIAL STAGE LOGIC CIRCUIT	03/31/98
4,999,519	SEMICONDUCTOR CIRCUIT WITH LOW POWER CONSUMPTION HAVING EMITTER-COUPLED LOGIC OR DIFFERENTIAL AMPLIFIER	03/12/91
6,031,365	BANDGAP REFERENCE USING A LOW VOLTAGE POWER SUPPLY	02/29/00
6,452,437	VOLTAGE GENERATOR FOR COMPENSATING FOR TEMPERATURE DEPENDENCY OF MEMORY CELL CURRENT	09/17/02
5,430,395	TEMPERATURE COMPENSATED CONSTANT-VOLTAGE CIRCUIT AND TEMPERATURE COMPENSATED CONSTANT CURRENT CIRCUIT	07/04/95

The Examiner's attention is respectfully directed to the following Foreign Patent Applications:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
JP404083405A	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	03/17/92
JP404095408A	SEMICONDUCTOR DEVICE	03/27/92
JP405055842A	SEMICONDUCTOR DEVICE	03/05/93

The Examiner's attention is respectfully directed to the following related pending U.S. patent applications:

CYPR-CD00196; "A NOVEL BAND-GAP CIRCUIT FOR PROVIDING AN ACCURATE REFERENCE VOLTAGE COMPENSATED FOR PROCESS STATE, PROCESS VARIATIONS AND TEMPERATURE"; 09/26/01; 09/964,991; Kutz et al.

CYPR-CD00197; "NOVEL POWER ON RESET CIRCUIT FOR A MICROPROCESSOR"; 06/22/01; 09/887,955; Kutz et al.

CYPR-CD00228; "APPARATUS AND METHOD FOR PROGRAMMABLE POWER MANAGEMENT IN A PROGRAMMABLE ANALOG CIRCUIT BLOCK" 08/29/01; 09/943,062; M. Mar

CYPR-CD00230; " A METHOD FOR EFFICIENT SUPPLY OF POWER TO A MICROCONTROLLER"; 09/922,579; 08/03/01; Kutz et al.

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